Progress on Digital Readout in DMILL

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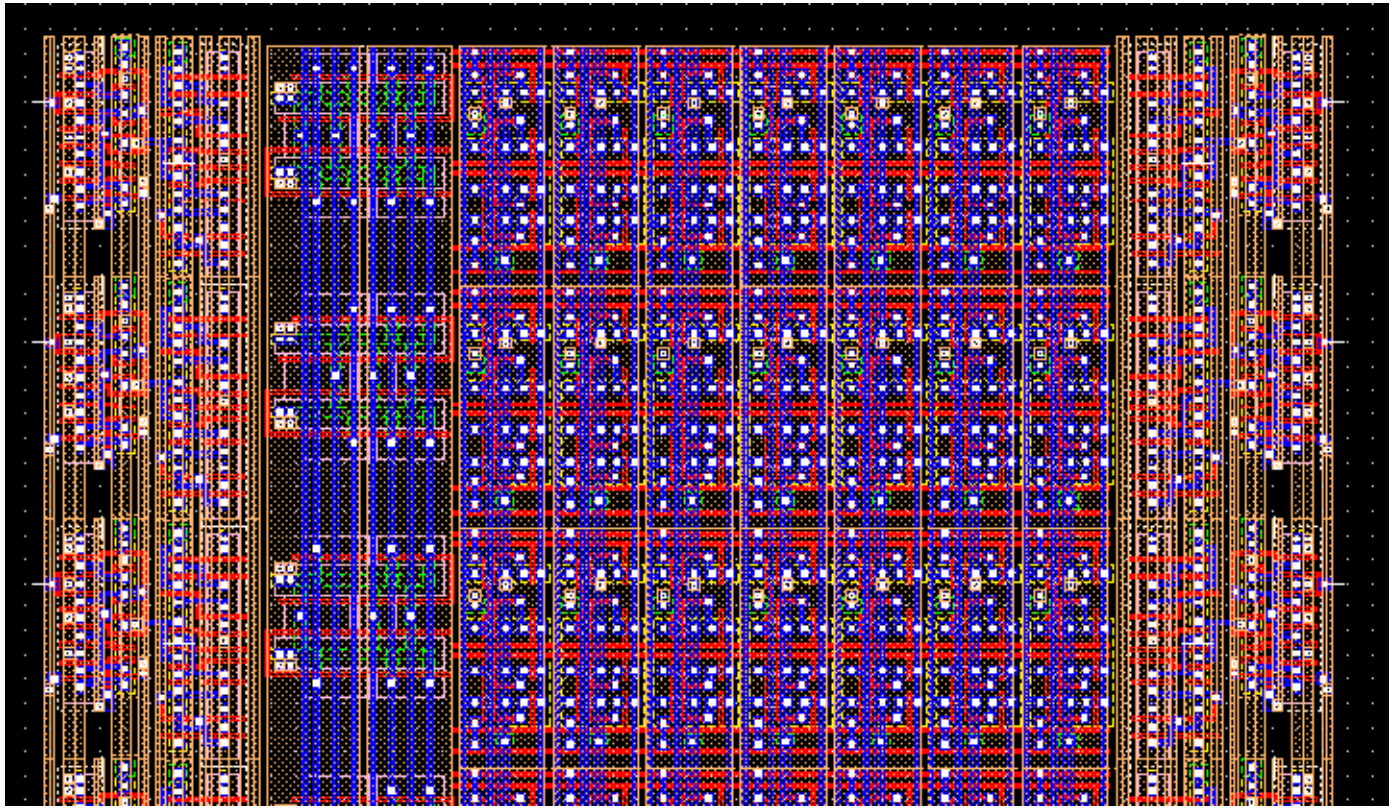
Overview of recent work for common DMILL "FE-D" chip at LBL...

Recent Work on Digital Readout Circuitry

Significant progress on DMILL layout:

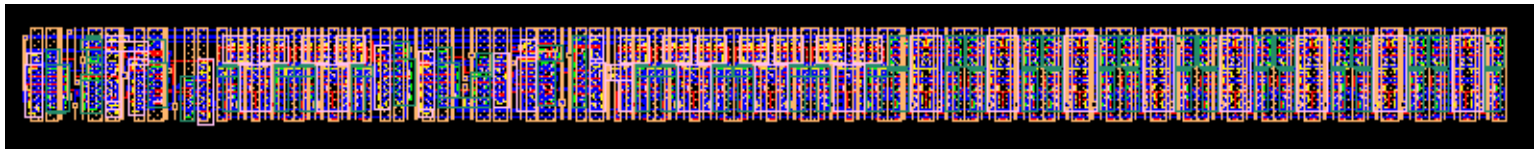
- Multiple iterations on pixel “back-end”, including single discriminator hit detection logic, LE + TE RAMs, ADDR ROM and sparse scan logic.
- Layout is complete for all blocks, no DRC’s within blocks. Present size is less than 170µ per pixel.

- Speed not yet optimized, so the size may grow slightly.

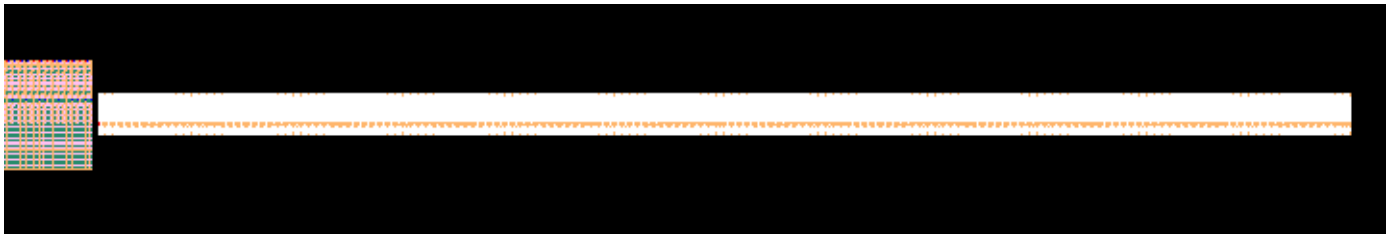


- Have made first pass through the EOC buffer. No major problems encountered, but further size optimization is being pursued.

- DRC not yet completely clean. Present size is 45µ by 760µ, but SRAM cell design still very conservative (12-T not 6-T). Should easily achieve old FE-B value (44µ by 685µ).



- Work proceeding on bottom of column design (sense amps plus arbitration logic). First “top160” assembly looks like:



- Still probably 1 month until the top160 block is complete and ready for full-scale SPICE simulations.

Verilog Work for DMILL Readout

Have begun serious work to allow Verilog simulation of complete readout logic:

- Back-annotating of blocks using HSPICE, then building up simulation of complete design using an abstract (neither gate-level nor behavioral) model.
- Also writing simplified functional description to provide expected output behavior (idealized description) to allow complete validation
- This should eliminate the types of errors which occured in FE-B.

Have also received “PM structures” from TEMIC:

- Simple transistor arrays, placed in dicing street on every wafer.
- Not complete enough to build SPICE model, but do allow checking of critical parameters.
- We will characterize, irradiate, and characterize again to check the reliability of the TEMIC DMILL BSIM3 models.
- TEMIC has more complete “test structures” which are like the drop-in “PM bars” which HP/MOSIS and Honeywell provide. We will also try to get some of these, but they are run infrequently...